REMARKS

Claims 1-44 and 50-52 are pending. These claims have been carefully reviewed and amended in certain instances to overcome the claim objections that were noted in the Office Action with respect to typographical errors. Accordingly, the claims objections should be withdrawn. The claims have also been amended to overcome the 35 U.S.C. 112, second paragraph rejection.

Claims 14-16, 18, 20-22, 36-39, 41-44, 50 and 52 are rejected as being anticipated under 35 U.S.C. 102(e) by LeBlanc et al, U.S. Patent 6,055,653 (LeBlanc). Further, claims 1-13, 31 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy et al (Roy), U.S. Patent 6,499,121 in view of Momohara, U.S. Patent 6,094,733. Still further, claim 17 is rejected as being unpatentable over LeBlanc in view of Ito et al (Ito), U.S. Patent 5,635,832. Reconsideration of the rejections is requested for the following reasons.

The apparatus and method of the present invention enables memory modules to be tested with respect to memory devices or modules that are used as a reference for the test by checking the relationship between the output signals of the memory modules to be tested and the reference memory modules. In particular, with reference to Fig. 1, memory modules to be tested are plugged into the sockets formed on performance

boards 3 in a constant temperature tank 7. A measurement PC unit 8 has, for example, a mother board 11 with a reference memory module 13, as shown in Fig. 2. A signal distribution unit 2 operates to receive the signal taken from the measurement PC 8 that has the mounted memory module 13 so that the signal can be used as a reference signal that is then distributed to the PFBs 3. A number of memory modules in the PFBs 3 can be tested simultaneously according to the present invention. In particular, a pass/fail signal can be taken out from the register 56 of the PFBs 3 to show the result of the test data, as shown in Fig. 9.

As shown in Fig. 1 and discussed in the specification, the cabinet in which the PFBs 3, the PC unit 1, the signal distribution unit 2, the display unit 4 and the power source 5 are contained can be separate from the cabinet in which the control PC 6 is contained. See page 16, lines 6-10 of the specification. Accordingly, the data processing unit having a memory that is used for the standard is mounted separately from the socket in which the memory device to be tested is mounted. As a result, the test apparatus of the present invention can replace the high speed tester of the prior art at a low cost. Further, the tester uses a personal computer that can be replaced cost effectively after a characteristic short service life.

With respect to LeBlanc, claims 14 and 36 and 52 have been amended to clarify that the terminal supplied with a data processing unit has a memory that is mounted separately from the socket or board that is mounted with a memory device to be tested. In LeBlanc, the gang SIMM memory tester is a printed wiring assembly (PWA) 201 that plugs into a single CPU SIMM slot such as slot 146 shown in Fig. 2B. A plurality of gang SIMMs 201, 213, 215, 217 are provided on the CPU board and, as shown in Fig. 3A, the gold SIMM 226 is provided close to the tester's edge connecter 320 to ensure signal integrity from the memory box 105. Address, data and control signals from memory bus 105 are received by gold SIMM 316 and then buffered, to fan out in parallel as discussed with reference to Fig. 4. Accordingly, the memory devices to be tested and the standard memory device used for the testing are mounted on the same board, which is different from the present invention in which the memory device to be tested is mounted on a socket or a board and the standard memory device is mounted separately from the socket or board on which the memory device to be tested is mounted. Therefore, LeBlanc does not anticipate claims 14-16, 18, 20-22, 36-39, 41-44, 50 and 52, and therefore the 35 U.S.C. 102(e) rejection should be withdrawn.

With respect to claims 1-13, 31 and 51, these claims are patentable over Roy in view of Momohara for the following

reasons. In particular, Roy discloses a system for testing a number of integrated circuits having an interface circuitry coupled to a single or multi-channel tester for receiving data values from the tester and providing error information concerning the devices under test (DUTs). The interface circuitry forwards data values that are received from the tester over a single channel to a number of DUTs in parallel. Error values resulting from the comparison using the data values read from the DUTs are returned to the tester. Roy does not disclose that part of the claimed invention which is directed to supplying at least one signal to a memory device to be tested and to a reference memory device in connection with the checking of the relationship between the output signals produced from the reference memory device and the output signals produced from the memory device to be tested. Further, the Momohara reference does not overcome the deficiency in Roy in this respect.

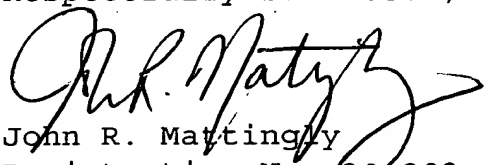
Specifically, Momohara discloses a tester that is designed to test a semiconductor memory device in which the tester executes the function test of a memory cell array and then performs redundancy analysis to replace abnormal portions of a memory cell array with a spare row/column. There is no disclosure of supplying a memory device to be tested with at least one signal that is supplied to the reference memory device and checking a relationship between the output signals

produced from the reference memory device and the output signals produced from the memory device to be tested, as claimed by Applicants in claim 1, for example, therefore, the combination of Roy and Momohara does not render the invention as claimed unpatentable over 35 U.S.C. 103(a).

Claim 17 has been rejected over LeBlanc in view of Ito, however, Ito is deficient with respect to disclosing the memory device testing apparatus of the present invention which includes a terminal supplied with a data processing unit having a reference memory device mounted separately from a socket that is to be mounted with a memory device to be tested. Accordingly, the combination of LeBlanc and Ito does not render the invention unpatentable under 35 U.S.C. 103(a) and therefore the rejection should be withdrawn.

In view of the foregoing amendments and remarks, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



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